DS1553

64kB, Nonvolatile, Year-2000-Compliant Timekeeping RAM

GENERAL DESCRIPTION

The DS1553 is a full-function, year-2000-compliant (Y2KC) real-time clock/calendar (RTC) with an RTC alarm, watchdog timer, power-on reset, battery monitor, and 8k x 8 nonvolatile static RAM. User access to all registers within the DS1553 is accomplished with a byte-wide interface as shown in Figure 1. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for day of month and leap year are made automatically.

Pin Configurations appear at end of data sheet.

FEATURES

- Integrated NV SRAM, RTC, Crystal, Power-Fail Control Circuit, and Lithium Energy Source
- Clock Registers are Accessed Identically to the Static RAM; These Registers are Resident in the 16 Top RAM Locations
- Totally Nonvolatile with Over 10 Years of Operation in the Absence of Power
- Precision Power-On Reset
- Programmable Watchdog Timer and RTC Alarm
- BCD-Coded Year, Month, Date, Day, Hours, Minutes, and Seconds with Automatic Leap Year Compensation Valid Up to the Year 2100
- Battery Voltage Level Indicator Flag
- Power-Fail Write Protection Allows for ±10% V_{CC} Power-Supply Tolerance
- Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time

ORDERING INFORMATION

PART	VOLTAGE (V)	TEMP RANGE	PIN-PACKAGE	TOP MARK**
DS1553-70	5.0	0°C to +70°C	28 EDIP (0.740)	DS1553-70
DS1553-70+	5.0	0°C to +70°C	28 EDIP (0.740)	DS1553+70
DS1553-100	5.0	0°C to +70°C	28 EDIP (0.740)	DS1553-100
DS1553W-120	3.3	0°C to +70°C	28 EDIP (0.740)	DS1553W-120
DS1553W-120+	3.3	0°C to +70°C	28 EDIP (0.740)	DS1553W+120
DS1553W-150	3.3	0°C to +70°C	28 EDIP (0.740)	DS1553W-150
DS1553P-70	5.0	0°C to +70°C	34 PowerCap®*	DS1553P-70
DS1553P+70	5.0	0°C to +70°C	34 PowerCap*	DS1553P+70
DS1553P-100	5.0	0°C to +70°C	34 PowerCap*	DS1553P-100
DS1553WP-120	3.3	0°C to +70°C	34 PowerCap*	DS1553WP-120
DS1553WP-120+	3.3	0°C to +70°C	34 PowerCap*	DS1553WP+120
DS1553WP-150	3.3	0°C to +70°C	34 PowerCap*	DS1553WP-150
DS9034PCX	3	0°C to +70°C	—	DS9034PCX

+ Denotes a lead-free/RoHS-compliant device.

**PowerCap required, must be ordered separately*

*** A "+" symbol anywhere on the top mark indicates a lead-free device.*

PowerCap is a registered trademark of Dallas Semiconductor.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +6.0V
Storage Temperature Range……..-40°C to +85°C
Soldering Temperature……...260°C for 10 seconds (DIP Package) (Note 8)
See IPC/JEDEC Standard J-STD-020A for Surface-Mount Devices

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

OPERATING RANGE

RANGE	TEMP RANGE	V_{CC}
Commercial	0°C to +70°C	3.3V ±10% or 5V ±10%

RECOMMENDED DC OPERATING CONDITIONS

(T_A = Over the operating range.)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 Voltage All Inputs	V_{CC} = 5V ±10%	V_{IH}	2.2		V_{CC} x +0.3V	V	1
	V_{CC} = 3.3V ±10%	V_{IH}	2.0		V_{CC} x +0.3V	V	1
Logic 0 Voltage All Inputs	V_{CC} = 5V ±10%	V_{IL}	-0.3		+0.8		1
	V_{CC} = 3.3V ±10%	V_{IL}	-0.3		+0.6		1

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = Over the operating range.)

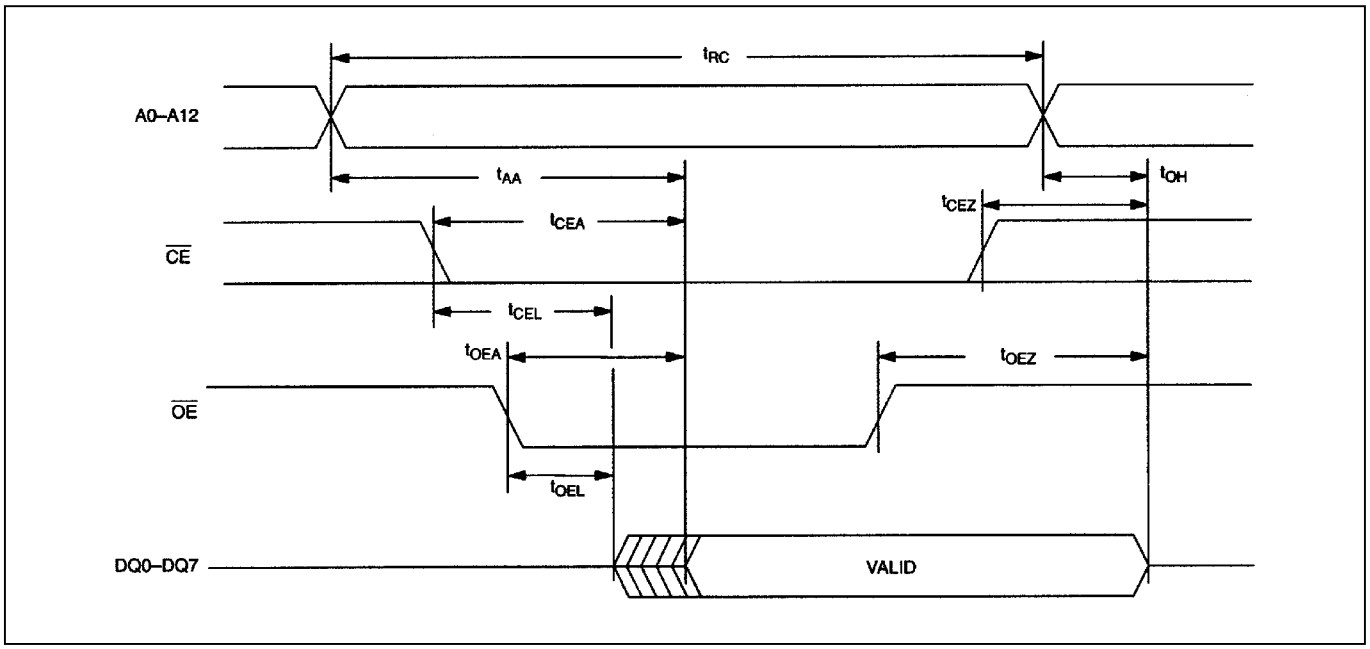
PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current		I_{CC}		15	50	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})		I_{CC1}		1	3	mA	2, 3
CMOS Standby Current ($\overline{CE} \geq V_{CC}$ - 0.2V)		I_{CC2}		1	3	mA	2, 3
Input Leakage Current (Any Input)		I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)		I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)		V_{OH}	2.4			V	1
Output Logic 0 Voltage	I_{OUT} = 2.1mA, DQ0-7 Outputs	V_{OL1}			0.4	V	1
	I_{OUT} = 7.0mA, $\overline{IRQ}$/FT and $\overline{RST}$ Outputs	V_{OL2}			0.4	V	1, 5
Write Protection Voltage		V_{PF}	4.20		4.50	V	1
Battery Switchover Voltage		V_{SO}		V_{BAT}		V	1, 4

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = Over the operating range.)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current		I_{CC}		10	30	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})		I_{CC1}		0.7	2	mA	2, 3
CMOS Standby Current ($\overline{CE}$ ≥ V_{CC} - 0.2V)		I_{CC2}		0.7	2	mA	2, 3
Input Leakage Current (Any Input)		I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)		I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)		V_{OH}	2.4			V	1
Output Logic 0 Voltage	I_{OUT} = 2.1mA, DQ0–7 Outputs	V_{OL1}			0.4	V	1
	I_{OUT} = 7.0mA, $\overline{IRQ}$/FT and $\overline{RST}$ Outputs	V_{OL2}			0.4	V	1, 5
Write Protection Voltage		V_{PF}	2.75		2.97	V	1
Battery Switchover Voltage		V_{SO}		V_{BAT} or V_{PF}		V	1, 4

Figure 5. Read Cycle Timing Diagram



READ CYCLE, AC CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = Over the operating range.)

PARAMETER	SYMBOL	70ns ACCESS		100ns ACCESS		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		ns	
Address Access Time	t_{AA}		70		100	ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5		5		ns	
$\overline{CE}$ Access Time	t_{CEA}		70		100	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}		25		35	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{OE}$ Access Time	t_{OEA}		35		55	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}		25		35	ns	
Output Hold from Address	t_{OH}	5		5		ns	

READ CYCLE, AC CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = Over the operating range.)

PARAMETER	SYMBOL	120ns ACCESS		150ns ACCESS		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	
Address Access Time	t_{AA}		120		150	ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5		5		ns	
$\overline{CE}$ Access Time	t_{CEA}		120		150	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}		40		50	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{OE}$ Access Time	t_{OEA}		100		130	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}		35		35	ns	
Output Hold from Address	t_{OH}	5		5		ns	

WRITE CYCLE, AC CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = Over the operating range.)

PARAMETER	SYMBOL	70ns ACCESS		100ns ACCESS		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Write Cycle Time	t_{WC}	70		100		ns	
Address Access Time	t_{AS}	0		0		ns	
$\overline{WE}$ Pulse Width	t_{WEW}	50		70		ns	
$\overline{CE}$ Pulse Width	t_{CEW}	60		75		ns	
Data Setup Time	t_{DS}	30		40		ns	
Data Hold time	t_{DH}	0		0		ns	
Address Hold Time	t_{AH}	5		5		ns	
$\overline{WE}$ Data Off Time	t_{WEZ}		25		35	ns	
Write Recovery Time	t_{WR}	5		5		ns	

WRITE CYCLE, AC CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = Over the operating range.)

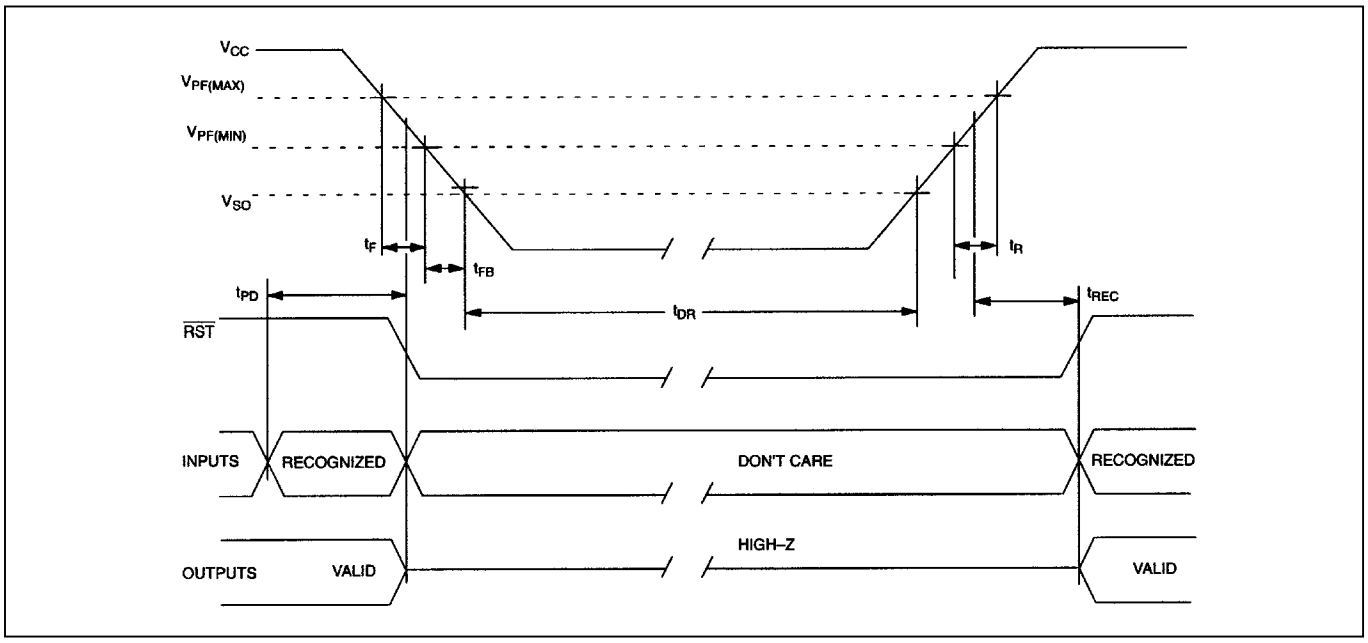
PARAMETER	SYMBOL	120ns ACCESS		150ns ACCESS		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Write Cycle Time	t_{WC}	120		150		ns	
Address Setup Time	t_{AS}	0		0		ns	
$\overline{WE}$ Pulse Width	t_{WEW}	100		130		ns	
$\overline{CE}$ Pulse Width	t_{CEW}	110		140		ns	
Data Setup Time	t_{DS}	80		90		ns	
Data Hold Time	t_{DH}	0		0		ns	
Address Hold Time	t_{AH}	0		0		ns	
$\overline{WE}$ Data Off Time	t_{WEZ}		40		50	ns	
Write Recovery Time	t_{WR}	10		10		ns	

POWER-UP/DOWN CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = Over the operating range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH}, Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Fall Time: $V_{PF(MIN)}$ to V_{SO}	t_{FB}	10			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
V_{PF} to $\overline{RST}$ High	t_{REC}	40		200	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	6, 7

Figure 8. Power-Up/Down Waveform Timing 5V Device

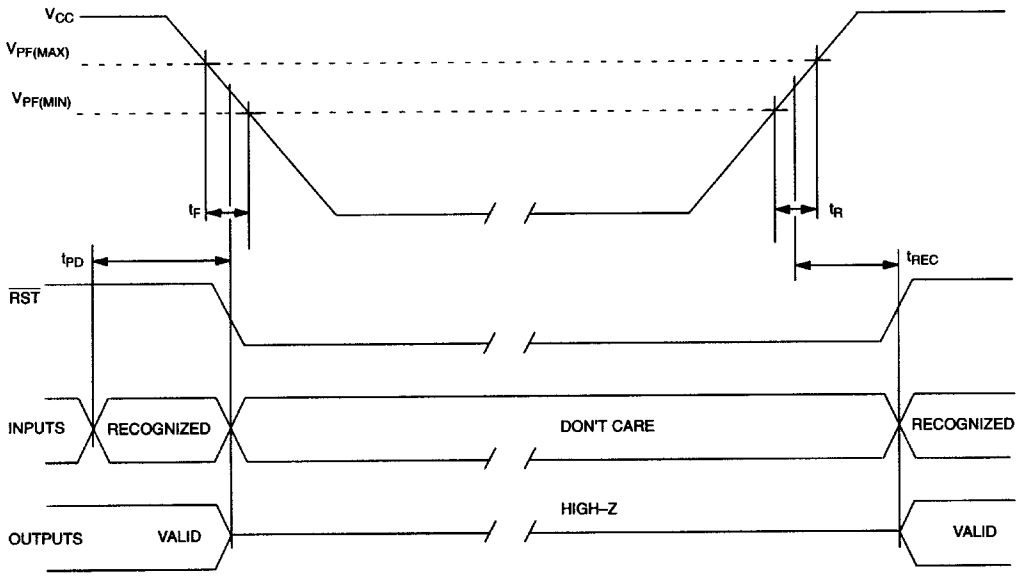


POWER-UP/DOWN CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = Over the operating range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH}, Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
V_{PF} to $\overline{RST}$ High	t_{REC}	40		200	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	6, 7

Figure 9. Power-Up/Down Waveform Timing 3.3V Device



CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on All Input Pins	C_{IN}			7	pF	1
Capacitance on $\overline{IRQ}$/FT, $\overline{RST}$, and DQ Pins	C_{IO}			10	pF	1

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 to 3.0V
Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

NOTES:

1) Voltage referenced to ground.
2) Typical values are at +25°C and nominal supplies.
3) Outputs are open.
4) Battery switch over occurs at the lower of either the battery voltage or V_{PF}.
5) The $\overline{IRQ}$/FT and $\overline{RST}$ outputs are open drain.
6) Data retention time is at +25°C.
7) Each DS1553 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined for DIP modules as a cumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
8) Real-time clock modules (DIP) can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibration is not used.

In addition, for the PowerCap:

a. Dallas Semiconductor recommends that PowerCap Module bases experience one pass through solder reflow oriented with the label side up (“live-bug”).
b. Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflow and use a solder wick to remove solder.